

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERC United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

DATE MAILED: 02/10/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/611,544	07/01/2003	Kenneth K. Smith	10010715-3	4975
7590 02/10/2005			EXAMINER	
HEWLETT-PACKARD COMPANY			SMITH, BRADLEY	
Intellectual Property Administration P.O. Box 272400			ART UNIT	PAPER NUMBER
Fort Collins, C	· -		2829	

Please find below and/or attached an Office communication concerning this application or proceeding.

	•						
		Application No.	Applicant(s)				
Office Action Summary		10/611,544	SMITH ET AL.				
		Examiner	Art Unit				
		Bradley K. Smith	2824				
Period f	The MAILING DATE of this communication app	pears on the cover sheet with	the correspondence address				
A SH THE - Exte after - If th - If NO - Failt Any	IORTENED STATUTORY PERIOD FOR REPL' MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. e period for reply specified above is less than thirty (30) days, a repl o period for reply is specified above, the maximum statutory period v ure to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing led patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply y within the statutory minimum of thirty (3 vill apply and will expire SIX (6) MONTH , cause the application to become ABAN	y be timely filed 30) days will be considered timely. S from the mailing date of this communication. DONED (35 U.S.C. § 133).				
Status							
1)[\]	Responsive to communication(s) filed on <u>02 N</u>	ovember 2004					
2a)□	This action is FINAL . 2b)⊠ This action is non-final.						
3)	<u>-</u>						
,_	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
4) 🔀	Claim(s) <u>1-22</u> is/are pending in the application. 4a) Of the above claim(s) <u>15-22</u> is/are withdrawn from consideration. Claim(s) is/are allowed.						
احصار ٠							
5)							
`—	☑ Claim(s) is allowed. ☑ Claim(s) <u>1-5 and 9-14</u> is/are rejected.						
	Claim(s) 6-8 is/are objected to. Claim(s) are subject to restriction and/or election requirement.						
Applicat	ion Papers						
	The specification is objected to by the Examine	r					
	The specification is objected to by the Examiner. D) The drawing(s) filed on <u>01 July 2003</u> is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
الحصارك ا							
11)	1) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
	under 35 U.S.C. § 119						
·	•	mala altri con de la O.S. L. O.O. O. A.	40(-) (1) (0				
	Acknowledgment is made of a claim for foreign ☐ All b)☐ Some * c)☐ None of: 1.☐ Certified copies of the priority documents	-	19(a)-(d) or (f).				
	2. Certified copies of the priority documents	s have been received in App	lication No				
	3. Copies of the certified copies of the prior	ity documents have been re	ceived in this National Stage				
	application from the International Bureau						
* 5	See the attached detailed Office action for a list	of the certified copies not red	ceived.				
•							
Attachmen 1\⊠ Notic	t(s) e of References Cited (PTO-892)	,, □,,,,	(DTO 440)				
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4) ∟_∟ Interview Sum Paper No(s)/M	mary (PTO-413) lail Date				
3) 🛛 Inforr	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date 7/1/03.		mal Patent Application (PTO-152)				

Art Unit: 2824

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species I in the reply filed on 11/02/04 is acknowledged.

Claims 15-22 are withdrawn from further consideration pursuant to 37 CFR
 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 11/02/04.

Priority

3. If applicant desires benefit of a previously filed application under 35 U.S.C. 121, specific reference to the earlier filed application must be made in the instant application. For benefit claims under 35 U.S.C. 120, 121 or 365(c), the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of the applications. This should appear as the first sentence(s) of the specification following the title, preferably as a separate paragraph unless it appears in an application data sheet. The status of nonprovisional parent application(s) (whether patented or abandoned) should also be included. If a parent application has become a patent, the expression "now Patent No. ______" should follow the filing date of the parent application. If a parent application has become abandoned, the expression "now abandoned" should follow the filing date of the parent application.

Specification

Art Unit: 2824

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: The method of making multiple logic bits per memory cell in a memory device.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 6. Claims 1-5 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lowrey et al. (US Patent 6,314,014). Lowrey et al. disclose providing a semiconductor substrate; forming electrically conductive columns on the semiconductor substrate; forming electrically conductive rows crossing over the electrically conductive columns (see figures 2a-2d); forming a plurality of memory components each having a resistance value corresponding to multiple logical bits (different resistance values)(see column 1 lines 30-60); and forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column. With regards to claim 2, Lowrey et al. disclose a component is formed to have a resistance value based on a thickness of electrically resistive material that forms an individual memory component (thickness is a component of volume)(see

Art Unit: 2824

column 1). With regards to claim 3, Lowery et al. disclose component is formed to have a resistance value based on an area of electrically resistive material that forms an individual memory component (by definition thickness x area = volume) (see column 1). With regards to claim 4, Lowery et al. disclose the component is formed to have a resistance value based on a shape (volume) of electrically resistive material that forms an individual memory component (see column 1). With regards to claim 5, Lowery et al. disclose the memory components are each formed to have a different resistance value based on a different area of electrically resistive material that forms a memory component (see column 1 lines 35-45). With regards to claim 14, Lowrey et al. disclose many layer of non-volatile memory cells (see figure 2A).

Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al. (US Patent 6,314,014) in view of Dill et al. (US Patent 6,114,719). Lowrey et al. disclose providing a semiconductor substrate; forming electrically conductive columns on the semiconductor substrate; forming electrically conductive rows crossing over the electrically conductive columns (see figures 2a-2d); forming a plurality of memory components each having a resistance value corresponding to multiple logical bits

(different resistance values)(see column 1 lines 30-60); and forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column. However Lowrey et al. fail to disclose forming a resistor element in series with a diode. Whereas Dill et al. disclose the forming a resistor element in series with a diode. Therefore it would have been obvious to one of ordinary skill at the time the invention was made to combine the teachings of Lowrey et al. and Dill et al. because the diode would make sure that current would only go one way through the resistor.

Page 5

9. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al. (US Patent 6,314,014) in view of Apodaca et al. (US Pre-grant Publication 2003/0122170).). Lowrey et al. disclose providing a semiconductor substrate; forming electrically conductive columns on the semiconductor substrate; forming electrically conductive rows crossing over the electrically conductive columns (see figures 2a-2d); forming a plurality of memory components each having a resistance value corresponding to multiple logical bits (different resistance values)(see column 1 lines 30-60); and forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column. However Lowrey et al. fail to disclose changing the resistance value with light or heat. Whereas Apodaca et al. disclose that phase-change material's resistance values may be changed though light or heat (see paragraph 0016). Therefore it would have been obvious to one of ordinary skill at the time the invention was made to combine the teachings of Lowrey et al. and Apodaca et al. because one would be able

Art Unit: 2824

to control the resistance value of phase change materials and would make the it easier for a manufacturer to control that variable in devices.

Allowable Subject Matter

- 10. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 11. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record neither teaches nor suggest within the context of the entire claim the components are each formed to have a resistance value based on a rectangular geometric shape of electrically resistive material that forms a memory component, at least some of the rectangular geometric shapes having different resistance values corresponding to an area of a rectangular geometric shape (claim 6), forming a first memory cell having a memory component that indicates logical bits 00 (zero-zero); forming a second memory cell having a memory indicates logical bits 01 (zero-one); component that forming a third memory cell having a memory component that indicates logical bits 10 (one-zero); and forming a fourth memory cell having a memory indicates logical bits 11 (one-one) (claim 7), forming a first memory cell that

Art Unit: 2824

indicates logical bits 00 (zero-zero) corresponding to a first resistance value based on an area of electrically resistive material that forms a memory component in the first memory cell; forming a second memory cell that indicates logical bits 01 (zero-one) corresponding to a second resistance value based on an area of electrically resistive material that forms a memory component in the second memory cell; forming a third memory cell that indicates logical bits 10 (one-zero) corresponding to a third resistance value based on an area of electrically resistive material that forms a memory component in the third memory cell; and forming a fourth memory cell that indicates logical bits 1 1 (one-one) corresponding to a fourth resistance value based on an area of electrically resistive material that forms a memory component in the fourth memory cell (claim 8).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tajiri (US pregrant publication 2004/0090815) disclose a non-volatile variable resistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is (571) 272-1884. The examiner can normally be reached on 10-6 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brad Smith

Primary Examiner

Art Unit 2829